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PATENT APPLICATION

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Date of Deposit: **June 8, 2000**

Signature: Teresa M. Hanlin

APPLICANT(S): Stephen V. Kosonocky

TITLE: Dynamic Adder With Reduced Logic

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Enclosed are the following papers relating to the above-named application for patent:

Application - 12 pages of Specification, 5 pages of Claims and 1 page of Abstract
5 Sheets of informal drawing(s)
Declaration and Power of Attorney
Assignment and Recordation Form Cover Sheet
Check in the amount of $808.00 to cover the filing fee and Assignment recordation fee

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	20-20 =	0	x $18 =	$0
Independent Claims	4-3 =	1	x $78 =	$78
Multiple Dependent Claim(s), if applicable			$260 =	$0
Basic Fee				$690
			TOTAL FEE:	$768

Please file the application and please find enclosed a check in the amount of $808.00 (which includes $768 to cover the filing fee and $40 to cover the Assignment recordation fee). In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Ryan & Mason, L.L.P. Deposit Account No. 50-0762** as required to correct the error. Duplicate copies of this letter are enclosed.

Please address all correspondence to: **William E. Lewis, Ryan & Mason, L.L.P., 90 Forest Avenue, Locust Valley, New York 11560**. Telephone calls should be made to the under-signed attorney at (516) 759-2946.

Respectfully,

William E. Lewis

William E. Lewis
Reg. No. 39,274
Attorney for Applicant(s)

Date: June 8, 2000
Ryan & Mason, L.L.P.
90 Forest Avenue
Locust Valley, New York 11560

DYNAMIC ADDER WITH REDUCED LOGIC

Field of the Invention

The present invention relates generally to logical adders and, more particularly, to a dynamic parallel adder which eliminates positive or negative complementary carry generate and propagate signal logic normally used to implement a conventional dynamic parallel adder.

Background of the Invention

A 64 bit adder function is typically the most basic frequency limiting function in a 64 bit microprocessor. Propagating information from a carry input to the most significant bit of the adder's operand is typically the longest logical delay path in the adder. Carry look-ahead schemes have been developed to reduce the total number of logic stages in this path at the expense of added logic.

Dynamic circuit realizations have also been shown to decrease the logic delay through the adder by reducing the total gate capacitance in each logic gate by the use of precharge signals and elimination of complementary logic transistors, but at the expense of an increase in the amount of logic gates, requiring both positive true and positive complement carry signals to be generated before computation of the final sum. Greater use of digital logic for accomplishing a specific function increases the circuit area resulting in increased cost and power usage.

As is known, "positive true" logic is defined as logic which outputs a signal which is electrically at a high voltage level (e.g., V_{DD}) when the function being evaluated by the logic is evaluated as "true" (e.g., a logical '1' state). On the other hand, "positive complement" logic is defined as logic which outputs a signal which is electrically at a high voltage level (e.g., V_{DD}) when the function being evaluated by the logic is evaluated as "complement" (e.g., a logical '0' state). Of course, dynamic logic may be implemented in terms of "negative true" and "negative complement" logic. As is known,

"negative true" logic is defined as logic which outputs a signal which is electrically at a low voltage level (e.g., V_{SS}) when the function being evaluated by the logic is evaluated as "true" (e.g., a logical '1' state). On the other hand, "negative complement" logic is defined as logic which outputs a signal which is electrically at a low voltage level (e.g., V_{SS}) when the function being evaluated by the logic is evaluated as "complement" (e.g., a logical '0' state). While positive or negative dynamic logic may be employed in an adder function, the descriptions herein refer to positive dynamic logic.

Thus, typical dynamic adder configurations are implemented with positive true block generate and block propagate signals, and also positive complementary versions of block generate and block propagate, to allow creating a final sum using an XOR (exclusive OR) logic circuit which is typically implemented as:

$$S(n) = (\text{^}p(n)*C(n-1) + (p(n)*\text{^}C(n-1)) \quad (1)$$

$$p(n) = a(n) + b(n), \quad (2)$$

where C(n-1) is the generate signal from bit (n-1), p(n) is the propagate signal from bit n and a(n), b(n) are two operand bits, ^ is the COMPLEMENT operator, * is the AND operator, + is the OR operator. It is to be understood that the COMPLEMENT operator ^ refers to the normal logical operation of complementing a signal, as opposed to the term "positive complementary" used with respect to dynamic circuit technology. In any case, it is known that the above representation of the final sum in equation (1) requires both a positive true and positive complementary version of C(n-1), where the positive complementary version of C(n-1) is constructed from positive complementary block generate and block propagate logic, to allow a dynamic implementation of this logic function. This stems from the requirement that dynamic logic gates require all inputs to either remain at a logic "0" state or transition only once to a logical "1" state, within a single clock cycle.

Summary of the Invention

The present invention provides an improved implementation of a binary dynamic adder. Specifically, in one aspect of the invention, a binary dynamic adder uses the following boolean expression for implementing the final sum:

$$S(n) = \wedge(p(n) * C(n-1))*(p(n) + C(n-1)). \quad (3)$$

The terms for evaluating the final sum bit are constructed from only positive (or negative) true block generate and block propagate signals, eliminating roughly half the carry logic associated with positive (or negative) complementary signal generation of the typical configuration. Expressing the final sum bit in the above form allows a simple implementation using a reduced number of dynamic logic gates, as will be explained in detail below and illustrated in accordance with the figures.

In another aspect of the invention, an *N*-bit parallel adder comprises: (i) a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute generate signals and propagate signals for each bit; (ii) a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage; (iii) a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and (iv) a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and

the summation signal is generated without the need for positive (or negative) complementary signal generation.

By eliminating the need for positive (or negative) complementary signal generation in the parallel adder, the invention provides many benefits. For example, the invention realizes the benefits of reduced power consumption and reduced circuit area due to the elimination of positive (or negative) complementary carry logic.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a schematic drawing of an XOR function according to an embodiment of the present invention constructed without the need for a positive complementary version of one of its inputs, using a combination of dynamic and static logic;

FIG. 2 is a schematic drawing of a dynamic logic gate according to an embodiment of the present invention used for grouping six carry signals to form a group six carry generate signal;

FIG. 3 is a schematic drawing of a dynamic logic gate according to an embodiment of the present invention used for grouping six carry propagate signals to form a group six carry propagate signal;

FIG. 4 is schematic drawing of a dynamic logic gate according to an embodiment of the present invention used to perform a sum calculation using a combination of group generate and propagate signals; and

FIG. 5 is a block diagram of a 64 bit parallel adder according to an embodiment of the present invention showing the connections between logical gates to transmit and forward carry terms which allow complete sum calculation in a minimum of logical calculations.

Detailed Description of Preferred Embodiments

In the following detailed description, certain specific terminology will be employed for the sake of clarity and a particular embodiment, but it is to be understood that the specific terminology is not intended to be limiting and should not be so construed inasmuch as the invention is capable of taking many forms and variations within the scope of the claims.

Further, while the following detailed description of illustrative embodiments of the invention refers to positive dynamic logic (requiring only positive true signal generation), one of ordinary skill in the art will realize that the principles of the invention may be applied to negative dynamic logic (requiring only negative true signal generation) in a straightforward manner.

The logical architecture of a preferred adder is based on the associative operator described in R. Brent and H.T. Kung, "A Regular Layout for Parallel Adders," IEEE Transactions on Computers, Vol. C-31, No. 3, March 1982, pp. 260-264, the disclosure of which is incorporated by reference herein, which allows reorganization of carry generate and propagate signals to reduce the maximum number of logical delay stages to propagate the carry signal. The sum bit for binary addition is given as:

$$s_i = a_i \oplus b_i \oplus c_{i-1} \qquad i = 1 \rightarrow n, \tag{4}$$

where a represents a first binary value and b represents a second binary value, i represents the bit number and $\oplus$ represents the summing operator. The carry signal, c_{i-1}, can be described in terms of generate and propagate signals as:

$$c_i = g_i + (p_i\, c_{i-1}), \tag{5}$$

where

$$g_i = a_i\, b_i \tag{6}$$

and

$$p_i = a_i \oplus b_i. \tag{7}$$

As described by Brent and Kung, an associative operator o can be defined that takes the form of:

$$(g, p)o(g', p') = g + (pg'), pp') \tag{8}$$

where

$$(G_i, P_i) = \begin{cases} (g_1, p_1) & if\ (i = 1) \\ \{(g_i, p_i)o(G_{i-1}, P_{i-1}) & if\ (2 \le i \le n) \end{cases} \tag{9}$$

Expansion of equation (9) and rearranging terms in a convenient manner, based on the associative property of the new operator, it is possible to construct an adder using $O(\log n)$ stages, where each stage takes the form of equation (8).

Greater reduction of logical delay stages can be obtained by combining multiple generate and propagate terms in a single complex logic stage. High frequency operation is possible if the generate-propagate stages are implemented with dynamic logic, exploiting the wide "or" structures available in this logic family, grouping together terms from multiple bits into group terms. As an example of grouping generate-propagate stages and minimizing the logic for implementation using dynamic circuits, expansion of equation (9) for n=6 and combining terms gives:

$$grpG_6 = G_6 + P_6G_5 + P_6P_5G_4 + P_6P_5P_4G_3 + P_6P_5P_4P_3G_2 + P_6P_5P_4P_3P_2G_1 \tag{10}$$

and

$$grpP_6 = P_6P_5P_4P_3P_2P_1, \tag{11}$$

where $grpG_6$ and $grpP_6$ are group generate and group propagate signals, respectively.

The high order product terms can be reduced using the relations:

$$Z = A + B + C + (DE) + (DF) + (DG), \tag{12}$$

$$Z = (A + B + C) + D\,(E + F + G) \tag{13}$$

$$Z = (A + B + C + D)\,(A + B + C + E + F + G), \tag{14}$$

using the boolean property that:

$$X + YZ = (X + Y)(X + Z). \tag{15}$$

Using the relations given by equation (12) through equation (15), equation (10) can be rewritten as:

$$\begin{aligned} grpG_6 = \quad & (G_6 + P_6G_5 + P_6P_5G_4 + P_6P_5P_4) \\ & (G_6 + P_6G_5 + P_6P_5G_4 + G_3 + P_3G_2 + P_3P_2G_1) \end{aligned} \tag{16}$$

The logical form of equation (16) is convenient for dynamic circuit implementation because it can be constructed with two complex "AND-OR" terms combined with a static NOR gate, where the partial product terms are no greater then three, which means the highest NMOS (negative MOS) transistor stack is three. A circuit realization of equation (16) is shown in FIG. 2. The first complex "AND-OR" term is represented by the logic configuration including transistors 4 through 14. Transistor 2 gates the clock signal. The second complex "AND-OR" term is represented by the logic

configuration including transistors 18 through 36. Transistor 16 gates the clock signal. The two complex "AND-OR" terms are combined via the NOR gate 38 to yield $grpG_6$.

Likewise, the large AND structure for equation (11) can be constructed with two "AND-OR" dynamic terms combined with a static NOR gate to create the wide "AND" function. A circuit realization of equation (11) using the described technique is shown in FIG. 3. The first "AND-OR" term is represented by the logic configuration including transistors 42 through 46. Transistor 40 gates the clock signal. The second "AND-OR" term is represented by the logic configuration including transistors 50 through 54. Transistor 48 gates the clock signal. The two "AND-OR" terms are combined via the NOR gate 56 to yield $grpP_6$. Similar reductions can be made for lower order generate-propagate terms which lead to:

$$grpG_5 = (G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4P_3)(G_5 + P_5G_4 + P_5P_4G_3 + P_3G_2 + P_3P_2G_1) \quad (17)$$

$$grpP_5 = P_5P_4P_3P_2P_1, \quad (18)$$

$$grpG_4 = (G_4 + P_4G_3 + P_4P_3)(G_4 + P_4G_3 + G_2 + P_2G_1), \quad (19)$$

$$grpP_4 = P_4P_3P_2P_1, \quad (20)$$

$$grpG_3 = G_3 + P_3G_2 + P_3P_2G_1, \quad (21)$$

$$grpP_3 = P_3P_2P_1, \quad (22)$$

$$grpG_2 = G_2 + P_2G_1, \quad (23)$$

$$grpP_2 = P_2P_1, \quad (24)$$

$$grpG_1 = G_1, \tag{25}$$

$$grpP_1 = P_1. \tag{26}$$

Dynamic circuit implementations of lower order group generate and group propagate terms given by equation (17) through equation (26) can be realized in a similar manner to that given for the highest level term given by equation (16) and implemented with the circuit in FIG. 2 and FIG. 3 with a reduction of inputs.

Calculation of the final sums is given by equation (4), where $c_{i-1} = g_{i-1}$. When used for merging nodes on the first level of the adder, the uppercase G, P's are replaced by the lower case values (g, p) obtained from the initial generate-propagate stage described by equation (6) and equation (7). Choice of the degree of generate-propagate merging, determines the maximum number of complex logic levels needed to fully propagate the generate-propagate terms. The degree of merging is balanced with the maximum fan-in and fan-out per adder node. This needs to be balanced with the CMOS (complementary metal oxide semiconductor) circuit technology available, trading off logic levels as a function of wire loading and power.

A high degree of merging (i.e., six), performed in the first two stages of the adder leaves the last stage with relatively smaller requirements on fan-in. This reduced requirement on the final generate-propagate stage allows combining this stage with the sum stage given by equation (4). A simple sum term, where the previous generate signal describes the complete carry term to that point can be given as:

$$s_i = G_{i-1} \oplus p_i. \tag{27}$$

Implementation of the "XOR" function with dynamic logic can be accomplished using the following boolean expansion:

$$A \oplus B = \left(\overline{AB}\right)(A + B). \tag{28}$$

Equation (28) can be implemented using a complex dynamic gate as shown in FIG. 1.

The operation of the logic gate described by equation (3) and shown in FIG. 1 works in the following manner. Initially, a low asserted reset signal applied to the clk pin activates transistor d11 and d14 which forces the voltages at nodes n11 and n12 to the high level and resets the output S(n) to a low level, while inputs C(n-1) and p(n) are reset to a low state cutting off transistors d12, d13, d15 and d16. At a later time, the reset signal attached to the clk pins is deasserted to a high level, cutting off the reset transistors d11 and d14, placing the nodes n11 and n12 into a high impedance dynamic state charged to a high voltage level. If input pins C(n-1) and p(n) are simultaneously asserted high, the output S(n) remains in a low logic level. If C(n-1) and p(n) remain at a low logic level, the output remains at a low logic level. If only one input C(n-1) or p(n) transition to a high logic level, the output will transition to a high logic level.

A sum node merging three prior group generate signals can be written as:

$$s_i = [G_{i-1} + P_{i-1}G_{i-2} + P_{i-1}P_{i-2}G_{i-3}] \oplus p_i. \tag{29}$$

The "XOR" can be expressed in the form given in equation (28) to produce:

$$s_i = \left[\overline{p_i G_{i-1} + p_i P_{i-1} G_{i-2} + p_i P_{i-1} P_{i-2} G_{i-3}}\right][G_{i-1} + P_{i-1} G_{i-2} + P_{i-1} P_{i-2} G_{i-3} + p_i]. \tag{30}$$

Inspection of equation (30) shows that the third sum term contains four product terms, this requires a stack of four NMOS transistors to implement with dynamic logic and is shown in FIG. 4. The first "AND-OR" term is represented by the logic configuration including transistors 60 through 70. Transistor 58 gates the clock signal. The second

"AND-OR" term is represented by the logic configuration including transistors 74 through 84. Transistor 72 gates the clock signal. Transistors 86 and 88 provide the complementing of the first term. The two "AND-OR" terms are combined via transistors 90 through 96 to yield s_i. Similar expressions can be constructed for simpler sum terms that require less combinations of previous generate-propagate terms.

A top level diagram of the 64 bit adder with a maximum fan-in of six, using the above logical expressions for each node is illustrated in FIG. 5. FIG. 5 shows the diagram of a 64 bit add function completed in four levels of complex logic stages. The first complex logical stage of the adder, labeled "g,p gen" in FIG. 5, computes the standard generate and propagate signals for each bit following equation (6) and equation (7). The next level, labeled "L1 G,P", computes the block generate and propagate signals for groups of one through six bits, as illustrated in FIG. 5. The fan-in to each node is limited to six for every sixth bit. Each node implements the functions described by equation (10), equation (11) or equation (17) through equation (26), depending on the fan-in requirements. The third level of the adder, labeled "L2 G,P" in FIG. 5, combines the block generate and propagate of the lower groups of six, with those higher groups of six bit blocks as shown in FIG. 5, using the same logical equations equation (10), equation (11) or equation (17) through equation (26). Nodes with a single input, pass through the generate and propagate signals with delay elements. The final and fourth complex logical stage, labeled "L3 G,P & sum" in FIG. 5, combines the remaining uncombined block generate and propagate signals (i.e., block generate and propagate signals which have not been combined in the previous stages) with each propagate bit given by equation (7), and generates the sum calculation using the boolean expression given by equation (30), dropping input terms when they are not applicable.

Accordingly, as has been explained above, the present invention provides a dynamic parallel adder which eliminates the positive (or negative) complimentary carry generate and propagate signal logic normally used to implement a conventional dynamic parallel adder. The method for implementing the inventive adder uses a novel XOR

configuration constructed with dynamic CMOS logic circuits. It is to be appreciated that the implementation of the 64 bit adder shown in FIGs. 1 through 5 and described by equation (16) through equation (30) is but one example of a 64 bit parallel dynamic adder circuit according to the invention, and those skilled in the art will recognize that this example is scaleable to higher and lower bit widths and different circuit styles. For example, the dynamic adder of the present invention may be implemented by discrete logic components, as part of an integrated circuit, or some combination thereof. The dynamic adder of the present invention may also be integrated as part of a microprocessor or some other processing device.

Although illustrative embodiments of the present invention have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be affected therein by one skilled in the art without departing from the scope or spirit of the invention.

Claims

What is claimed is:

1. Apparatus for use in summing at least two binary values, comprising:

a binary adder circuit, responsive to a first binary value, a second binary value and a carry value, and operative to generate a binary output value representative of a summation of the first binary value, the second binary value and the carry value, the binary adder circuit having logic for implementing an exclusive OR function that generates the binary output value without one of a positive and a negative complementary version of the carry value.

2. The apparatus of claim 1, wherein the binary output signal S(n) is represented by an expression: ^(p(n) * C(n-1))*(p(n) + C(n-1)), where C(n-1) is a generate signal from a binary value n-1 associated with the carry value, p(n) is a propagate signal associated with the first binary value and the second binary value, ^ is a logical complement operator, * is an AND operator, and + is an OR operator.

3. The apparatus of claim 2, wherein the logic of the binary adder circuit comprises:

a first NMOS transistor stage for performing an AND operation on the generate signal and the propagate signal;

an inverter stage, coupled to the first NMOS transistor stage, for inverting an output signal generated by the first NMOS transistor stage;

a second NMOS transistor stage for performing an OR operation on the generate signal and the propagate signal; and

a NOR gate, coupled to the inverter stage and the second NMOS transistor stage, for combining an output signal generated by the inverter stage and an output signal generated by the second NMOS transistor stage to generate the binary output value.

4. The apparatus of claim 3, wherein the first NMOS transistor stage is responsive to more than one generate signal and more than one propagate signal.

5. The apparatus of claim 4, wherein the second NMOS transistor stage is responsive to more than one generate signal and more than one propagate signal.

6. An *N*-bit parallel adder, comprising:

a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without the need for one of positive and negative complementary signal generation.

7. The parallel adder of claim 6, wherein a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$, where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a represents the first binary value

and b represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

8. The parallel adder of claim 6, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

9. The parallel adder of claim 6, wherein the fourth logic stage implements an exclusive OR function to generate the summation signal.

10. The parallel adder of claim 9, wherein bit i of the summation signal is: $\left[\overline{p_i G_{i-1} + p_i P_{i-1} G_{i-2} + p_i P_{i-1} P_{i-2} G_{i-3}}\right] [G_{i-1} + P_{i-1} G_{i-2} + P_{i-1} P_{i-2} G_{i-3} + p_i]$, where p is a propagate signal and g is a generate signal and P is a group propagate signal and G is a group generate signal.

11. The parallel adder of claim 6, wherein N is equal to 64.

12. The parallel adder of claim 6, wherein the logic stages are implemented with complementary metal oxide semiconductor components.

13. A method of adding, in parallel, a first N-bit binary value and a second N-bit binary value, the method comprising the steps of:

computing generate signals and propagate signals for each bit;

computing block generate signals and block propagate signals for groups of one through m bits from the generate and propagate signals computed in the first computing step;

combining the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

combining remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and generating a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without the need for one of positive and negative complementary signal generation.

14. The method of claim 13, wherein a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$, where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a represents the first binary value and b represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

15. The method of claim 13, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

16. The method of claim 13, wherein the summation signal is generated in accordance with an exclusive OR function.

17. The method of claim 16, wherein bit i of the summation signal is: $\left[\overline{p_i G_{i-1} + p_i P_{i-1} G_{i-2} + p_i P_{i-1} P_{i-2} G_{i-3}}\right] [G_{i-1} + P_{i-1} G_{i-2} + P_{i-1} P_{i-2} G_{i-3} + p_i]$, where p is a propagate signal and g is a generate signal and P is a group propagate signal and G is a group generate signal.

18. The method of claim 13, wherein N is equal to 64.

19. The method of claim 13, wherein the computing, combining and generating steps are implemented with complementary metal oxide semiconductor components.

20. A processing device having an *N*-bit parallel adder, the *N*-bit parallel adder comprising:

a first logic stage, the first logic stage configured to receive a first *N*-bit binary value and a second *N*-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through *m* bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

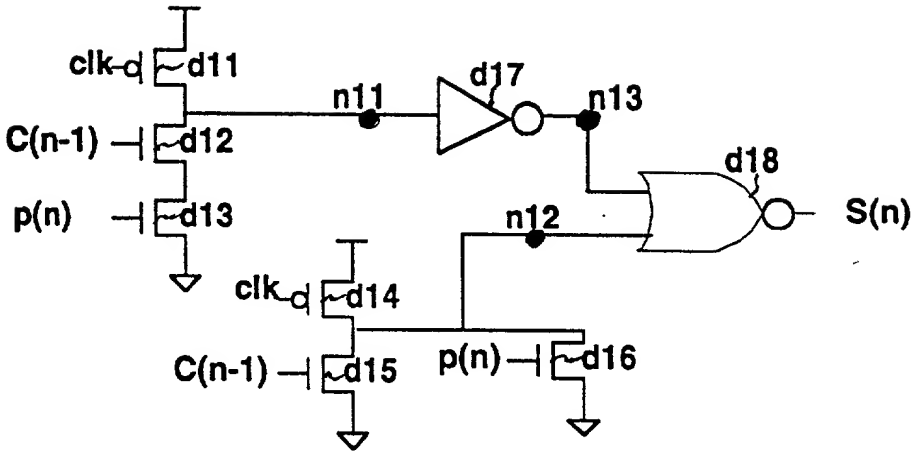
a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without the need for one of positive and negative complementary signal generation.

DYNAMIC ADDER WITH REDUCED LOGIC

Abstract of the Disclosure

A dynamic parallel adder is provided which eliminates the positive (or negative) complimentary carry generate and propagate signal logic normally used to implement a conventional dynamic parallel adder. The method for implementing the inventive adder uses a novel XOR configuration constructed with dynamic CMOS logic circuits.

1500-44.APP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n13
C(n-1)
d12
d18
p(n)
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n12
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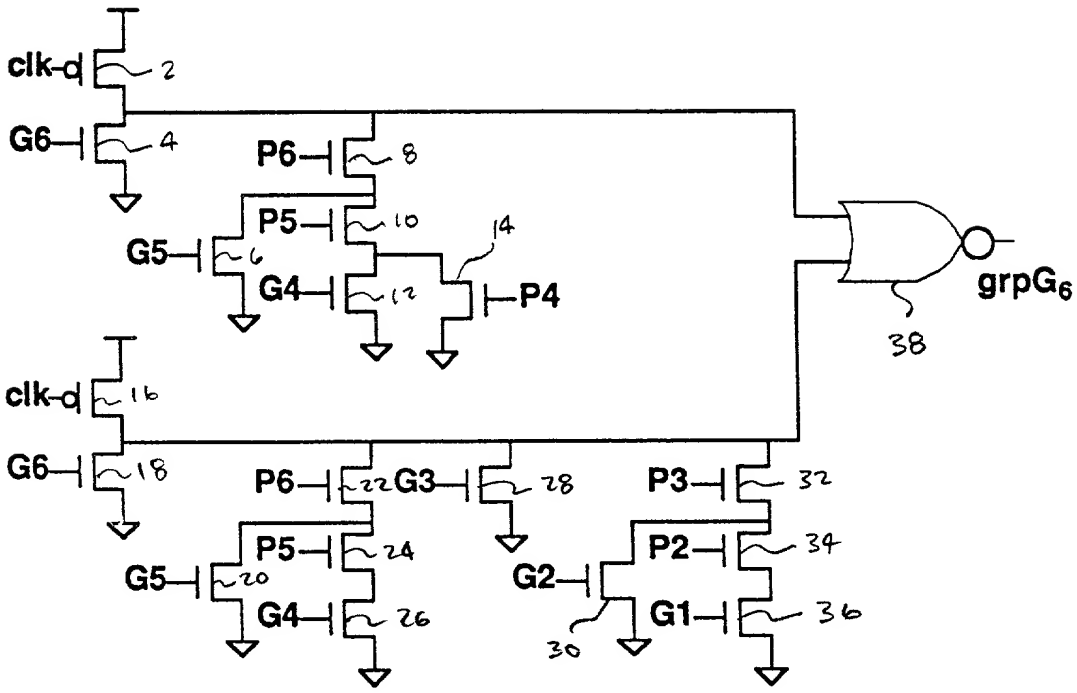
clk
d14
C(n-1)
d15
p(n)
d16

FIG. 1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16
G6
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P6
22
G3
28
P3
32
P5
24
P2
34
G5
20
G2
G4
26
30
G1
36

FIG. 2

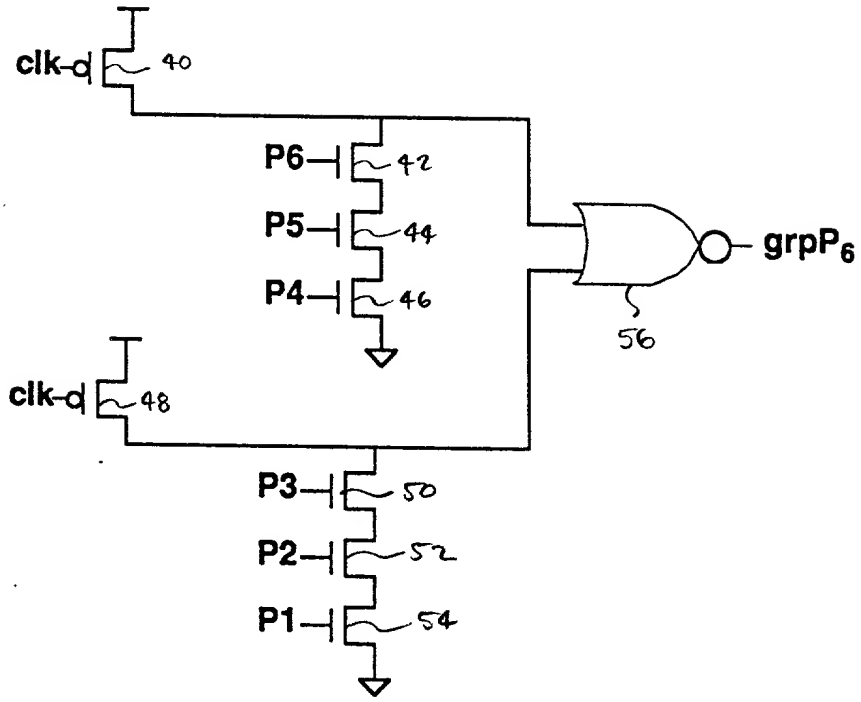

FIG. 3

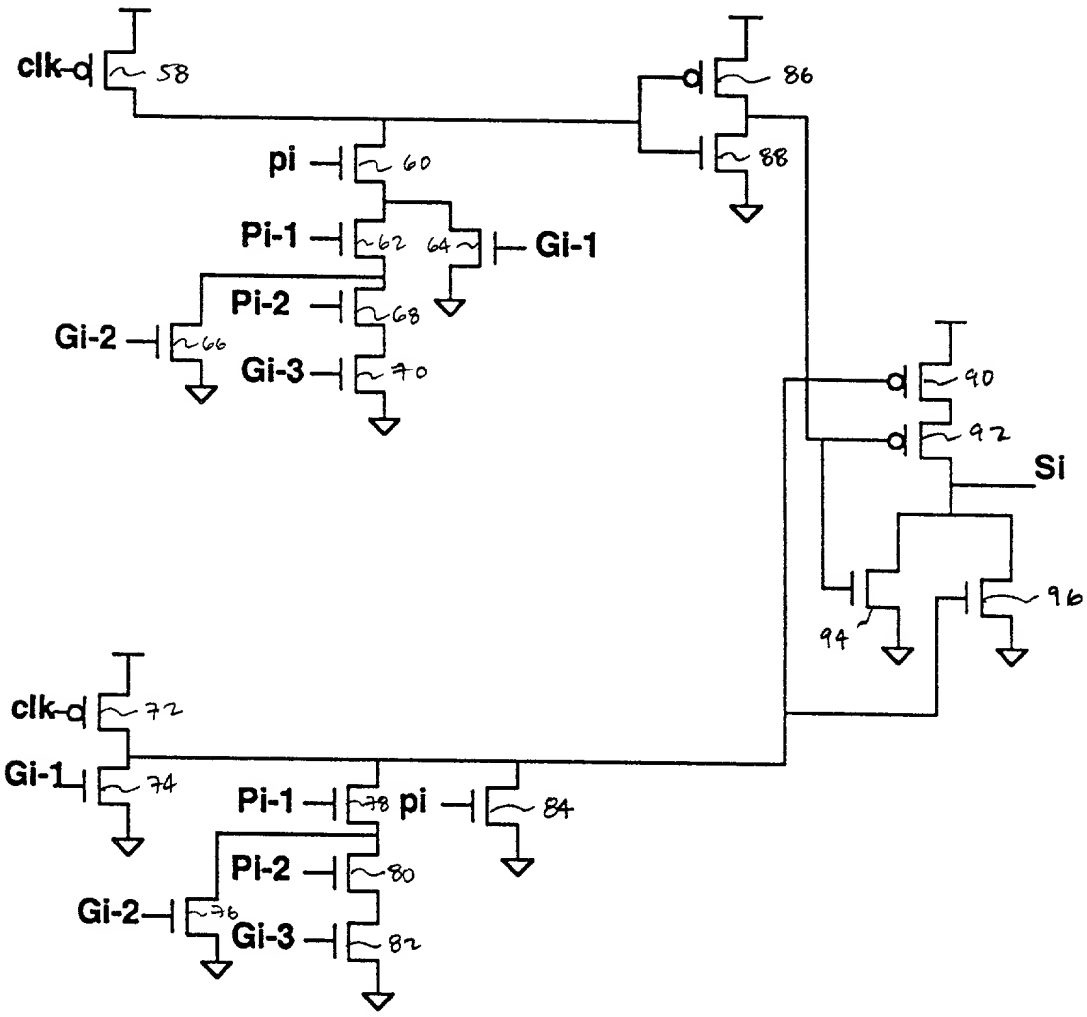
clk-d
58
pi
60
Pi-1
62
64
Gi-1
Pi-2
68
Gi-2
66
Gi-3
70
d
86
88
d
90
d
92
Si
94
96
clk-d
72
Gi-1
74
Pi-1
78
pi
84
Pi-2
80
Gi-2
76
Gi-3
82

FIG. 4

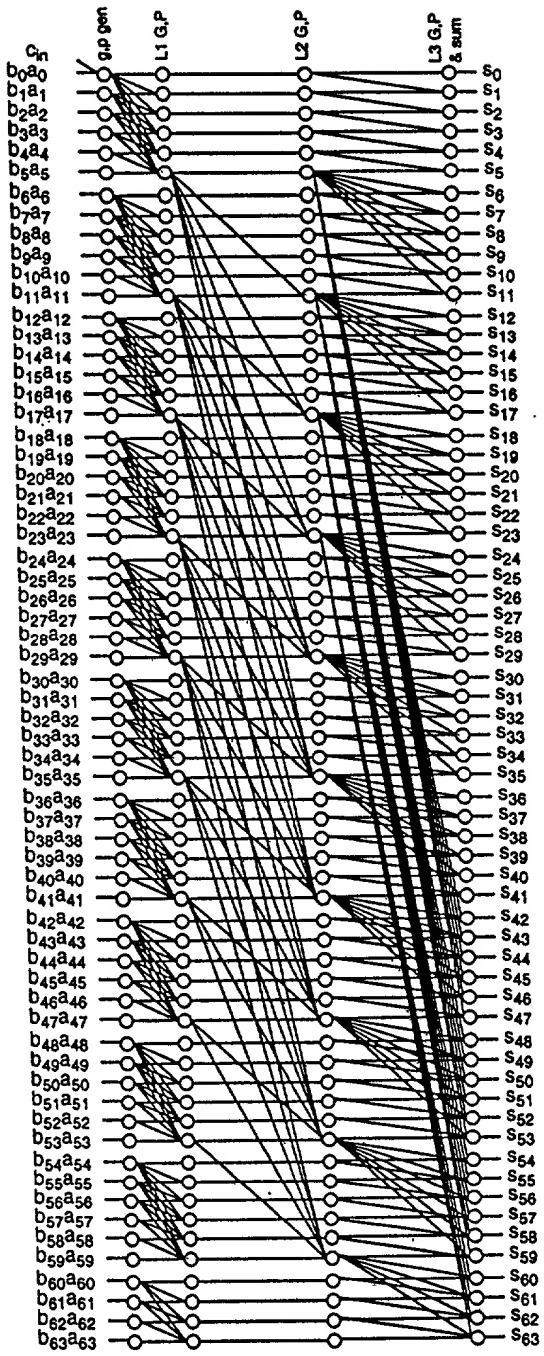
C_{in}
g,p gen
L1 G,P
L2 G,P
L3 G,P & sum
b_0a_0 b_1a_1 b_2a_2 b_3a_3 b_4a_4 b_5a_5 b_6a_6 b_7a_7 b_8a_8 b_9a_9 $b_{10}a_{10}$ $b_{11}a_{11}$ $b_{12}a_{12}$ $b_{13}a_{13}$ $b_{14}a_{14}$ $b_{15}a_{15}$ $b_{16}a_{16}$ $b_{17}a_{17}$ $b_{18}a_{18}$ $b_{19}a_{19}$ $b_{20}a_{20}$ $b_{21}a_{21}$ $b_{22}a_{22}$ $b_{23}a_{23}$ $b_{24}a_{24}$ $b_{25}a_{25}$ $b_{26}a_{26}$ $b_{27}a_{27}$ $b_{28}a_{28}$ $b_{29}a_{29}$ $b_{30}a_{30}$ $b_{31}a_{31}$ $b_{32}a_{32}$ $b_{33}a_{33}$ $b_{34}a_{34}$ $b_{35}a_{35}$ $b_{36}a_{36}$ $b_{37}a_{37}$ $b_{38}a_{38}$ $b_{39}a_{39}$ $b_{40}a_{40}$ $b_{41}a_{41}$ $b_{42}a_{42}$ $b_{43}a_{43}$ $b_{44}a_{44}$ $b_{45}a_{45}$ $b_{46}a_{46}$ $b_{47}a_{47}$ $b_{48}a_{48}$ $b_{49}a_{49}$ $b_{50}a_{50}$ $b_{51}a_{51}$ $b_{52}a_{52}$ $b_{53}a_{53}$ $b_{54}a_{54}$ $b_{55}a_{55}$ $b_{56}a_{56}$ $b_{57}a_{57}$ $b_{58}a_{58}$ $b_{59}a_{59}$ $b_{60}a_{60}$ $b_{61}a_{61}$ $b_{62}a_{62}$ $b_{63}a_{63}$
s_0 s_1 s_2 s_3 s_4 s_5 s_6 s_7 s_8 s_9 s_{10} s_{11} s_{12} s_{13} s_{14} s_{15} s_{16} s_{17} s_{18} s_{19} s_{20} s_{21} s_{22} s_{23} s_{24} s_{25} s_{26} s_{27} s_{28} s_{29} s_{30} s_{31} s_{32} s_{33} s_{34} s_{35} s_{36} s_{37} s_{38} s_{39} s_{40} s_{41} s_{42} s_{43} s_{44} s_{45} s_{46} s_{47} s_{48} s_{49} s_{50} s_{51} s_{52} s_{53} s_{54} s_{55} s_{56} s_{57} s_{58} s_{59} s_{60} s_{61} s_{62} s_{63}

FIG. 5

DECLARATION

AS A BELOW NAMED INVENTOR, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole (*if only one name is listed below*), or an original, first and joint inventor (*if plural names are listed below*), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE: **DYNAMIC ADDER WITH REDUCED LOGIC**

the specification of which is attached hereto or indicates an attorney docket no. YO999-369, or:

☐ was filed in the U.S. Patent & Trademark Office on _____ and assigned Serial No. _____,

☐ and (*if applicable*) was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability and to the examination of this application in accordance with Title 37, Code of Federal Regulations §1.56. I hereby claim foreign priority benefits under Title 35, U.S. Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States, or §119(e) of any United States provisional application(s), listed below and have also identified below any foreign applications for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Priority Claimed:

_____ Yes [ ] No[ ]

(*Application Number*) (*Country*) (*Day/Month/Year filed*)

_____ Yes [ ] No[ ]

(*Application Number*) (*Country*) (*Day/Month/Year filed*)

I hereby claim the benefit under Title 35, U.S. Code §120, of any United States application(s), or §365(c), of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International applications(s) in the manner provided by the first paragraph of Title 35, U.S. Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

_____

(*Application Serial Number*) (*Filing Date*) (*STATUS: patented, pending, abandoned*)

_____

(*Application Serial Number*) (*Filing Date*) (*STATUS: patented, pending, abandoned*)

I hereby appoint the following attorneys: **MANNY W. SCHECTER**, Reg No. 31,722; **TERRY J. ILARDI**, Reg. No. 29,936; **CHRISTOPHER A. HUGHES**, Reg. No. 26,914; **EDWARD A. PENNINGTON**, Reg No. 32,588; **JOHN E. HOEL**, Reg No. 26,279; **JOSEPH C. REDMOND, Jr.**, Reg No. 18,753; **DOUGLAS W. CAMERON**, Reg. No. 31,596; **STEPHEN C. KAUFMAN**, Reg No. 29,551; **JAY P. SBROLLINI**, Reg. No. 36,266; **WAYNE L. ELLENBOGEN**, Reg. No. 43,602; **ROBERT M. TREPP**, Reg. No. 25,933; **LOUIS P. HERZBERG**, Reg. No. 41,500; **LOUIS J. PERCELLO**, Reg. No. 33,206; **PAUL J. OTTERSTEDT**, Reg. No. 37,411; **DANIEL P. MORRIS,** Reg. No. 32,053; and **DAVID M. SHOFI,** Reg. No. 39,835; each of them of **INTERNATIONAL BUSINESS MACHINES CORPORATION**, Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598; to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or re-examination application, with full power of appointment and with full power to substitute an associate attorney or agent, and to receive all patents which may issue thereon, and request that all correspondence be addressed to:

William E. Lewis
RYAN & MASON, L.L.P.
90 Forest Avenue
Locust Valley, NY 11560
Tel.: (516) 759-2946

I HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE INVENTOR: Stephen V. Kosonocky Citizenship U.S.A.

Inventor's signature: Stephen V. Kosonocky Date: 6/7/00

Residence & Post Office address: 19 Lakeside Avenue
Darien, Connecticut 06820